NON-PROVISIONAL APPLICATION FOR U. S. PATENT UNDER 37 CFR 1.53(b) TRANSMITTAL FORM

Attorney Docket No. TI-29646

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

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Trish Paramore

For: Modulation Scheme for Filterless Switching Amplifiers

Enclosed are:

_3_ sheets of informal drawings and 12 pages of Specification (including Abstract)
_x_ A Declaration/Power of Attorney
_x_ Assignment with form PTO 1595

FEE CALCULATION					FEE
	NUMBER		**NUMBER EXTRA**	**RATE**	**BASIC FEE $ 760.00**
Total Claims	20	-20 =		X $18 =	$ .00
Independent Claims	2	- 3 =		X $78 =	$.00
				Total Filing Fee	$760.00

Please charge Deposit Account No. 20-0668 in the amount of the Total Fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0668.

All correspondence related to this application may be addressed to the undersigned at Christopher L. Maginniss at Texas Instruments Incorporated, M/S 3999, P.O. Box 655474, Dallas, TX 75265.

November 16, 1999
Date

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MODULATION SCHEME FOR FILTERLESS SWITCHING AMPLIFIERS

CROSS REFERENCE TO RELATED APPLICATIONS

Cross-reference is made to commonly assigned patent application entitled "Concept and Methods to Enable Filterless, Efficient Operation of Class-D Amplifiers," filed herewith, the teaching of which are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention is generally related to switching amplifier circuits, and more particularly to Class-D amplifiers.

BACKGROUND OF THE INVENTION

Switching amplifiers, also know as Class-D amplifiers as the name implies, have an output that is switched or pulse-width modulated (PWM) at a frequency much higher than the frequency of interest. For example, in audio applications, these amplifiers will switch at typical frequencies of 250kHz, while the audio band is limited to 20kHz. These amplifiers are analogous to switching regulators, and receive similar benefits and disadvantages of such devices when compared to their linear counterparts. The main advantage of these switching amplifiers is their efficiency and its derivatives, i.e., lower thermal dissipation, battery life, smaller power supplies, size, weight, etc. The main disadvantage is cost and complexity.

Present modulation schemes utilizing either half or full H-bridge output stage topologies which switch in a "binary" fashion. In such a switching method, there are two valid states for the bridge, neglecting dead time, which are shown at 10 in Figure 1 and Figure 2. Although simpler to implement, the disadvantage of this solution is that there is always a current 12 provided to the load due to the voltage differential always provided across nodes OUTP and OUTN, shown at 14, illustrated in Figure 3. For operation near zero crossing, or no audio signal, the majority of the current used is wasted, and is a drop in efficiency. As shown in Figure 3, an output squarewave with a 50% duty cycle will spend 50% of the time period decaying the current in the inductor, and 50% of the period to re-establish the current in the opposite direction, this resulting in a time averaged current of zero.

Furthermore, this will require that the load be inductive. Consider a pure resistive load. Switching the H-bridge in a "binary" fashion would place the power supply voltage across the load (plus parasitics of the switch). Unlike the current waveform 12 shown in Figure 3, the resulting current would be a squarewave with a magnitude equal to the power supply divided by the resistance of the load. For example, an H-bridge using a 5V supply driving a 4Ω load would see a current of about 1 Amp, and this is with no signal. Although the electrical equivalent of a speaker is somewhere between purely resistive and purely inductive, this would still prevent filterless operation of Class-D amplifiers in audio applications as the main benefit of efficiency is lost. Today, the problem is solved by providing some current limiting device in series with the speaker, usually a post-filter comprised of inductors and thereby creating a current flow shown at 12 in Figure 3. The typical circuit topology is shown at 16 in Figure 4.

SUMMARY OF THE INVENTION

The present invention acheives technical advantages as a circuit and a method achieving filterless Class-D operation, increased efficiency, and reduced cost by delivering current to the load only when needed, and once delivered, maintain the current by not decaying or wasting energy in removing the current. This is accomplished by using a terinary modulation scheme. This scheme is implemented in an H-bridge configuration, where there are four states of operation as the scheme implies. The modulation scheme generates PWM signals, whereby the edges of the voltage signal at a node OUTP move away from each other, and the edges of the voltage signal at a node OUTN move towards each other. The voltage difference of these two signals, which appears across the load, is narrow pulses. These pulses also have the desired affect of doubling the single-ended PWM frequency.

The present invention allows for filterless operation of Class-D amplifiers, which becomes a huge cost, board, and implementation savings. Cost of a filter for Class-D amplifier at least matches silicon cost, thus making Class-D solutions at least 2x solution cost more than their linear counterparts. Eliminating the filter is currently the only way to be cost competitive with linear amplifiers. Also, the modulation scheme allows for higher efficiency and reduced board space, where fractions of the filter can be used.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects of the invention including specific embodiments are understood by reference to the following detail description taken in conjunction with the detail drawings in which:

Figure 1 is a schematic diagram of a prior art Class-D switching amplifier operating in binary fashion depicting a first state of operation;

Figure 2 is a schematic diagram of the Class-D switching amplifier shown in Figure 1 depicting the second state of operation;

Figure 3 is a signaling diagram illustrating the voltage signals provided to the output terminals, a differential voltage delivered across the load, and the current conducted through the load;

Figure 4 is a schematic diagram of a typical post filter for the "binary" modulation scheme;

Figure 5 is a schematic diagram of a third state of operation of the present invention generating no voltage differential across the load;

Figure 6 is a schematic diagram of the present invention shown in Figure 5 illustrating a fourth state of operation of the present invention, also generating no voltage differential across the load, and thus no current through;

Figure 7 is a timing diagram illustrating the voltage signals at the output terminals, the differential voltage across the load and the current conducted through the load for the states of operation shown in Figure 5 and Figure 6; and

Figure 8 is a timing diagram of the present invention corresponding to the third and fourth states of operation depicted in Figure 5 and Figure 6 illustrating a differential voltage being generated across the load, and thus, a corresponding current.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention achieve technical advantages as a Class-D switching amplifier having four states of operation, the first two states being shown in Figure 1 and Figure 2, a third state of operation shown in Figure 5 at 20 and a fourth state of operation shown at 30 in Figure 6.

Referring to Figure 7 and Figure 8, there is shown two states of a terinary modulation scheme, a generated differential output voltage, and current waveforms according to the preferred embodiment of the present invention. As shown in Figure 5, controlling voltage signals controllably are provided by control circuit 21 to the four switching MOS transistors MP1, MN1, MP2, and MN2 in a switching sequence so as to alternate between the first state of operation shown in Figure 1, the second state of operation shown in Figure 2, the third state of operation shown in Figure 5 and the fourth state of operation shown in Figure 6.

As shown in Figure 7, a voltage waveform 22 and a voltage waveform 24 provided by the switches to the output terminals OUTP and OUTN, respectively,

and are in phase and correspond to one another in state 1 and state 2, thereby generating no differential voltage across the load as shown at 26, and thus, generating no current through the load as shown as 28.

Referring now to Figure 8, when it is desired to deliver current to the load corresponding to an input signal provided to control circuit 21, the control signals provided to the gates of the four switching MOS transistors MP1, MN1, MP2, and MN2 by controller 21 operate the switching circuit in states 3 and 4 as shown in Figure 5 and Figure 6, whereby this is done by moving the edges of the voltage signal 32 at terminal OUTP away from each other, and the edges of the voltage signal 34 towards each other. The difference of these two signals provided between output terminals OUTP and OUTN appear across the load L1 as narrow pulses, depicted at 35 of waveform 36. These pulses 35 have the desired effect of doubling the single-ended PWM frequency. Current does decay as the speaker and MOS switches MN1, MN2, MP1 and MP2 have resistive components that are lossy.

The Class-D amplifier and method of operation thereof achieves technical advantages as a filterless Class-D operation that has increased efficiency, and reduced cost by delivering current to the load only when needed, and furthermore, when once delivered, maintaining the current by reducing the rate of decay or decreasing the waste of energy in removing the current. The present invention achieves this using the terinary modulation scheme implemented in a H-bridge configuration having four states of operation, as shown in Figure 1, Figure 2, Figure 5, and Figure 6.

The present invention allows for filterless operation of Class-D amplifiers, which is a huge savings for design and component implementation. The present invention allows the cost of the improved Class-D amplifier to be more in line

with the costs of linear counterpart. The present invention eliminates the need for post switching circuit filters and is thus cost competitive with the linear amplifiers. The terinary modulation scheme allows for higher efficiency and reduced board space.

While the invention has been described in conjunction with preferred embodiments, it should be understood that modifications will become apparent to those of ordinary skill in the art and that such modifications are therein to be included within the scope of the invention and the following claims.

WE CLAIM:

1. A Class-D switching amplifier, comprising:

a first, second, third and fourth switch each having a respective control terminal, a first output terminal disposed between said first switch and said second switch, and a second output terminal disposed between said third switch and said fourth switch; and

a control circuit coupled to each said control terminals and pulse and width modulating (PWM) said four switches such that no voltage differential is generated between said first output terminal and said second output terminal in a first state of operation for a first predetermined time period.

2. The Class-D amplifier as specified in Claim 1 wherein said control circuit PWM controls said four switches such that a differential voltage is generated between said first output terminal and said second output terminal in a third state of operation for a second predetermined time period.

3. The Class-D switching amplifier as specified in Claim 2 wherein a current delivered to a load connected between said first output terminal and said second output terminal directly corresponds to the differential voltage therebetween.

4. The Class-D switching amplifier as specified in Claim 2 wherein the ratio of the first predetermined time period to the second predetermined time period is correlated to the voltage potential generated between the first and second output terminals.

5. The Class-D switching amplifier as specified in Claim 2 wherein the control circuit PWM controls said four switches in a second state generating no said voltage differential between said first output terminal and said second output terminal, and a fourth state generating a voltage differential between said first output terminal and said second output terminal, said switches being controlled differently in said first state than said third state, and said switches being controlled differently in said second state than said fourth state.

6. The Class-D switching amplifier as specified in Claim 4 wherein the average voltage provided across the first and second output terminals is a function of the ratio of the first predetermined time period to the second predetermined time period.

7. The Class-D switching amplifier as specified in Claim 2 further comprising a load coupled between said first and second output terminals.

8. The Class-D switching amplifier as specified in Claim 7 wherein said load has an inductive component.

9. The Class-D switching amplifier as specified in Claim 8 wherein said load is inductive.

10. The Class-D switching amplifier as specified in Claim 1 wherein the first and second switch are coupled in series between a first voltage potential and a second voltage potential, and said third switch and said fourth switch are coupled in series between said first voltage potential and said second voltage potential.

11. A Class-D switching amplifier, comprising:

a first switch and a second switch coupled in series between a first voltage potential and a second voltage potential, a third switch and a fourth switch coupled in series between said first voltage potential and said second voltage potential, a first output terminal defined between said first and second switches, a second output terminal defined between said third and fourth switches, each said switch having a control terminal; and

a control circuit coupled to each said control terminals pulse width modulating (PWM) said four switches such that no voltage differential is generated between said first output terminal and said second output terminal in a first state of operation for a first predetermined time period.

12. The Class-D switching amplifier as specified in Claim 11 wherein said control circuit PWM controls said four switches such that a differential voltage is generated between said first output terminal and said second output terminal in a second state of operation for a second predetermined time period.

13. The Class-D switching amplifier as specified in Claim 12 wherein a current delivered to a load connected between said first output terminal and said second output terminal directly corresponds to the differential voltage therebetween.

14. The Class-D switching amplifier as specified in Claim 12 wherein the ratio of the first predetermined time period to the second predetermined time period is correlated to the voltage potential generated between the first and second output terminals.

15. The Class-D switching amplifier as specified in Claim 12 wherein the control circuit PWM controls said four switches in a second state generating no said voltage differential between said first and second output terminals, and a fourth state generating a voltage differential between said first and second output terminals, said switches being controlled differently in said first state than said second state, and being controlled differently in said third state than said fourth state.

16. The Class-D switching amplifier as specified in Claim 14 wherein the average voltage provided across the first and second output terminals is a function of the ratio of the first predetermined time period to the second predetermined time period.

17. The Class-D switching amplifier as specified in Claim 12 further comprising a load coupled between said first and second output terminals.

18. The Class-D switching amplifier as specified in Claim 17 wherein said load has an inductive component.

19. The Class-D switching amplifier as specified in Claim 18 wherein said load is inductive.

20. The Class-D switching amplifier as specified in Claim 18 wherein the second voltage potential is ground and the first voltage potential is positive with respect to ground.

ABSTRACT

A Class-D switching amplifier (20) having a terinary modulation scheme implemented in an H-bridge configuration. The present invention has four states of operation, and achieves increased efficiency and reduced cost by delivering current to the load only when needed, and once delivered, maintaining the current. The Class-D switching amplifier eliminates the need for post amplifier filters.

TI-29646

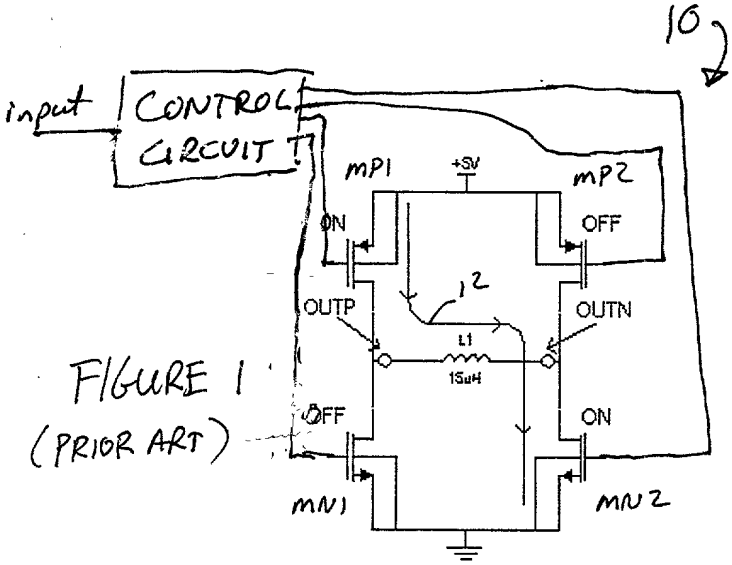

FIGURE 1
(PRIOR ART)

high-side OUTP On, low-side OUTN On

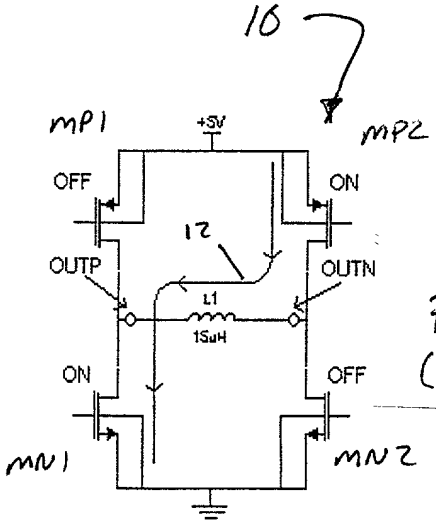

FIGURE 2
(PRIOR ART)

high-side OUTN On, low-side OUTP On

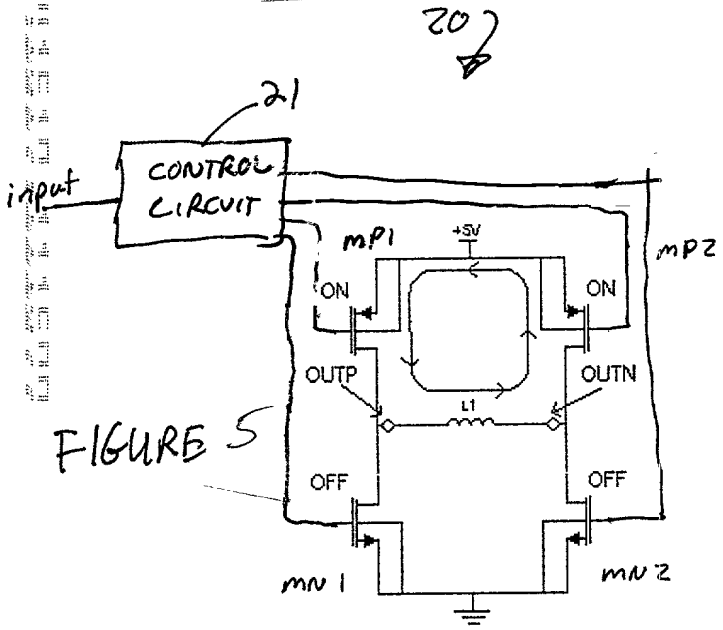

FIGURE 5

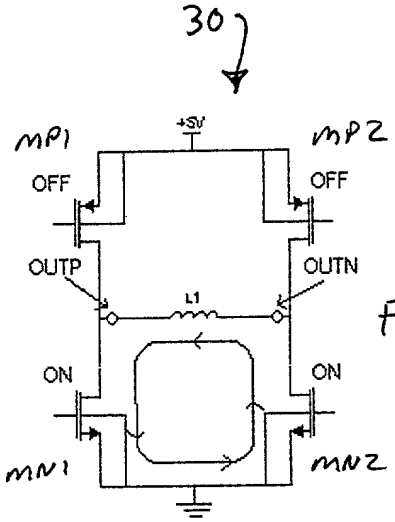

FIGURE 6

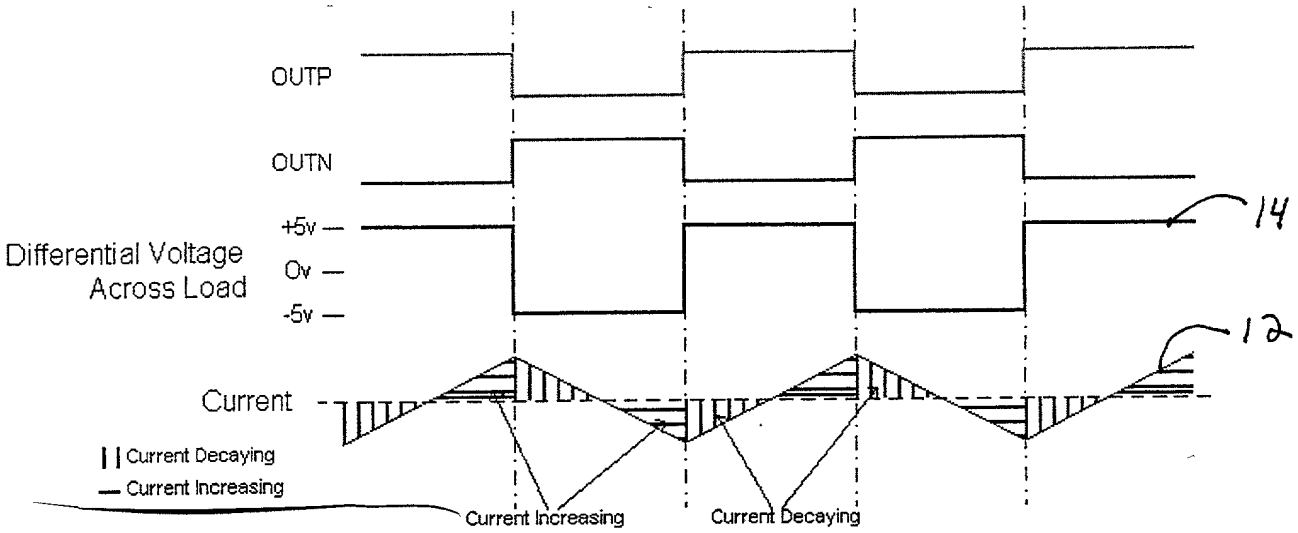

FIGURE 3
(PRIOR ART)

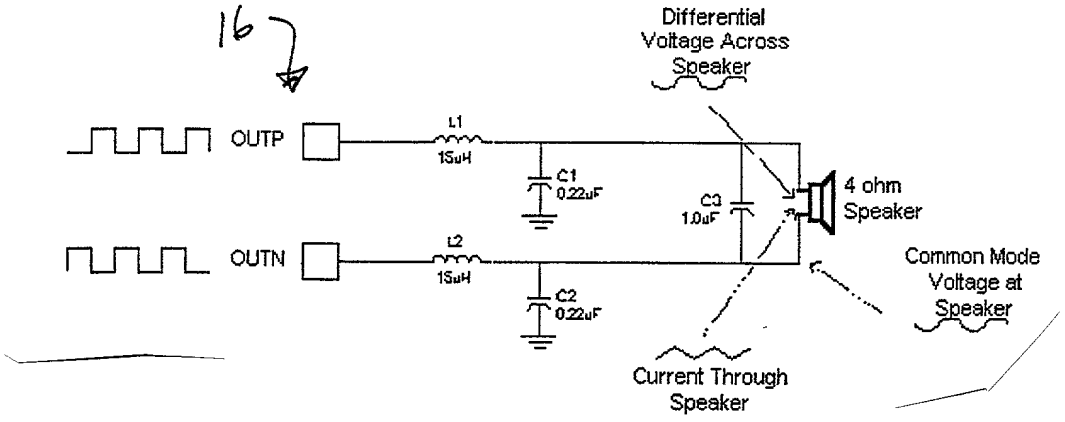

FIGURE 4
(PRIOR ART)

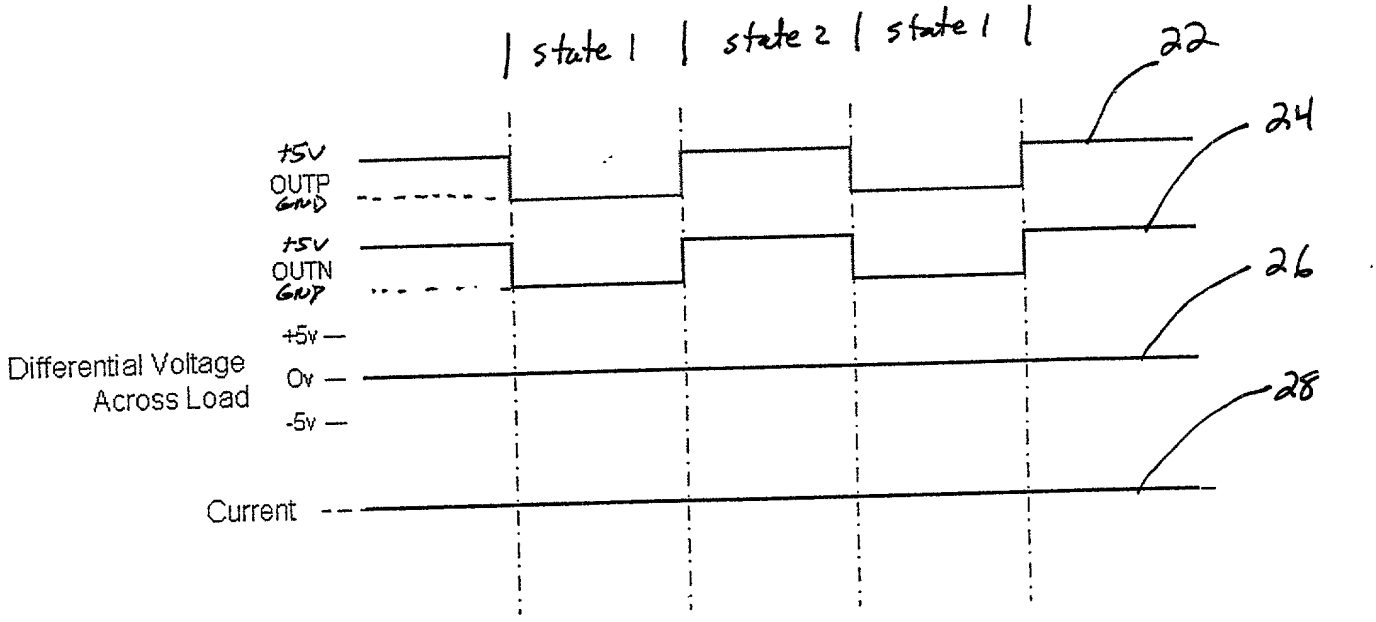

FIGURE 7

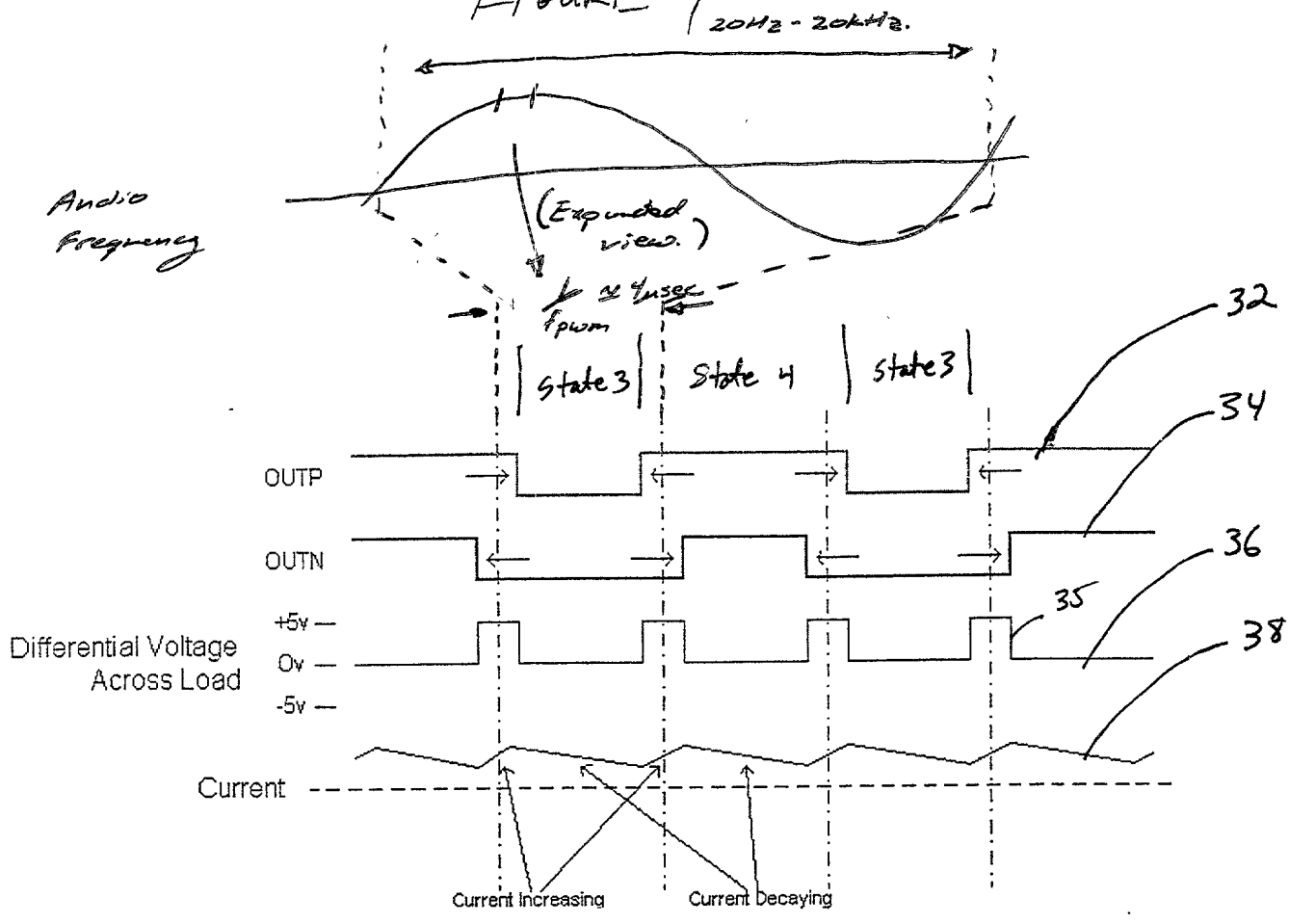

FIGURE 8

ATTORNEY'S DOCKET NO.

TI-29646

APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a);

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

MODULATION SCHEME FOR FILTERLESS SWITCHING AMPLIFIERS

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP: Great Britain	COUNTRY OF CITIZENSHIP: USA
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DATE: 9th November 1999	DATE: 9th November 1999	DATE: 12th November 1999

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DATE: 9th November 1999	DATE:	DATE: